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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,755	09/26/2003	Echere Iroaga	1847-US	9347

7590 09/20/2005

EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/20/2005

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,755	IROAGA, ECHERE	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-11 and 13* is/are rejected.

7)☒ Claim(s) *4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's amendment filed on 7/28/05 has been received and entered in the case. In view of newly discovered prior art, the previous rejections are now withdrawn and replaced with new grounds of rejection. Any inconvenience caused by the delay in citing this new prior art is regretted.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-4, 8, 11 and 13 are objected to because of the following informalities: the recitation of a common-source gain stage is incorrect, i.e., as shown in the instant drawings it is the drain of the parallel-connected transistors QP1 through QPN which are in common with each other. Note also claims 2-4 have the same problem. In claim 8, line 1, the word "the" should be inserted after the word wherein. In claims 11 and 13, the same problem exists with respect to the recitation of a common-source gain stage. Also in claim 11, line 3, "the output node" lacks antecedent basis. In claim 13, line 1, the word "and"

should be deleted and a comma is needed after the number "11". Appropriate correction is required.

4. Claims 1-3, 5-7, 9-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kono.

Note Figs. 6 and 12 of this reference which show, inter alia, an impedance divider (Fig. 6) having its output coupled to the input of a common-drain gain stage (the combination of the FETs between the current mirror and ground). The recited current mirror reads on the combination of transistors MP14 and MP15. The parallel array of programmable transistors reads on MN15, MN17, and mn19. The impedance divider of the claims is shown in Fig. 6, which includes resistance RLO, FET MP13, and FET MN13. The compensation signal is the output of Fig. 6, which is received by transistor MN14, and the compensation current is the current supplied to the input of FET MP14.

5. Claims 1-3, 5-7, 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaussi et al or Narendra et al.

Note Figs. 1a, 1b and Fig. 2 of Jaussi et al, and Figs. 1 and 2 of Narendra et al. These figures show all of

the limitations of the above-noted claims except for the impedance divider outputting a compensation signal to parallel-connected FETs. Such would have been obvious, however, because it is well-known in the art that resistors such as elements 214, 218, 222, etc in Figs. 2 of Jaussi et al and Narendra et al are commonly formed by biasing the gate of FETs with a constant bias voltage, such as that output from a common node of an impedance divider formed by a pair of resistors between high and low voltage levels of a power supply. The motivation for using this type of arrangement for forming the parallel resistors in Fig. 2 of Jaussi et al and Narendra et al is to provide a smaller structure, i.e., save real estate on the chip because integrated FET resistors are known in the art to be smaller than discrete resistor elements such as those of the two above-noted references.

6. Claims 4 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. In view of the above-noted new grounds of rejection not necessitated by applicant's amendments, this action is non-final.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to

the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

September 16, 2005